PROCEEDINGS OF SCIENCE

ATLAS ITk Strip Detector for High-Luminosity LHC

Jiri Kroll[*†]
Institute of Physics of the Czech Academy of Sciences, Prague, Czech Republic
E-mail: jiri.kroll@cern.ch

The ATLAS experiment is currently preparing for an upgrade of the tracking system in the course of the High-Luminosity LHC that is scheduled for 2026. The radiation damage at the expected integrated luminosity of $4000\,\mathrm{fb}^{-1}$ and hadron fluencies over $2\times10^{16}\,\mathrm{n_{eq}/cm^2}$ requires a replacement of existing Inner Detector by an all-silicon Inner Tracker with a pixel detector surrounded by a strip detector. The ATLAS ITk detector will enable to bring Level-0 trigger rate of a few MHz down to a Level-1 trigger rate below 1 MHz at the peak instantaneous luminosity of $7.5\times10^{34}\,\mathrm{cm^{-2}s^{-1}}$ that corresponds to approximately 200 inelastic proton-proton interactions per beam crossing. The current prototyping phase, that is working with ITk Strip Detector consisting of a four-layer barrel and a forward region composed of six disks on each side of the barrel, has resulted in the ATLAS Inner Tracker Strip Detector Technical Design Report, which starts the pre-production readiness phase at the involved institutes. In this contribution we present the design of the ITk Strip Detector and current status of R&D of various detector components.

The 26th International Workshop on Vertex Detectors
10-15 September, 2017
Las Caldas, Asturias, Spain

*Speaker.
†On behalf of the ATLAS Collaboration

PoS(Vertex 2017)008

1. Introduction

The current ATLAS Inner Detector (ID) was designed for 10 years of operation at the instantaneous luminosity of 1.0×10^{34} cm^{-2}s^{-1}, 14 TeV centre-of-mass energy, 25 ns time between individual beam crossings and the average pile-up of 23 proton-proton interactions per beam crossing, with the front-end architecture based on the single hardware trigger signal running at a peak rate of 100 kHz [1]. However, the scientific programme of the LHC spans over the next 20 years and includes an ambitious series of upgrades that will ultimately result in the installation of High-Luminosity LHC (HL-LHC) accelerator, that will deliver very high peak instantaneous luminosities of $5.0 - 7.5 \times 10^{34}$ cm^{-2}s^{-1} corresponding to approximately 200 inelastic proton-proton interactions per beam crossing, with an accumulated integrated luminosity for proton-proton collisions of 4000 fb^{-1}. The HL-LHC will thus present an extremely challenging environment to the ATLAS experiment, well beyond that for which it was designed.

The radiation-hard silicon sensors and electronics used in current ATLAS ID were designed to withstand the radiation damage that is equivalent to the integrated luminosity of 400 fb^{-1} in case of current Pixel detector, 700 fb^{-1} for Semi-Conductor Tracker (SCT) and 850 fb^{-1} for innermost B-layer. Above the designed fluences the intrinsic hit efficiencies drop below the limits required for efficient pattern recognition [2] and the leakage currents from the detectors will both exceed the limits on power supplies and the capacity of the cooling system. The front-end electronics of both the Pixel and SCT detectors can accommodate events with about 50 proton-proton interactions per beam crossing which come with sustained instantaneous luminosity of 2.0×10^{34} cm^{-2}s^{-1}. As it is discussed in Ref. [2], already for an average number of superimposed minimum bias events in each beam crossing of 70 at a Level-1 rate of 100 kHz much of the innermost strip barrel cannot be read out. With 200 proton-proton interactions per beam crossing inside the current detector the efficiency of the patern recognition and the track-finding efficiency will be compromised by the confusion due to additional hits without compensating increase in granularity. The current ID does not provide any tracking information to the existing first level hardware trigger system. It was shown in [2] that by adding the tracking information to the trigger objects provided by the calorimeters and muon system, trigger thresholds could be lowered which directly benefits the physics performance. All these limitations necessitate the complete replacement of the current ID by an all-silicon ITk for the Phase-II upgrade of the ATLAS experiment.

2. Design of ATLAS ITk detector

To satisfy the requirements on physics studies, tracking performance and material distribution in X_0 at HL-LHC the ATLAS ITk detector design combines significant increase of detector granularity and data bandwidth with high mechanical stability, unprecedented radiation hardness and low material budget, see Figure 1.

2.1 ITk Strip layout

In the central region of the ITk the individual detector modules are arranged in the cylinders around the beam axis, with five pixel layers followed by two short-strip and two long-strip layers of paired stereo modules. The forward regions will be covered by six end-cap (EC) strip disks and

PoS(Vertex 2017)008

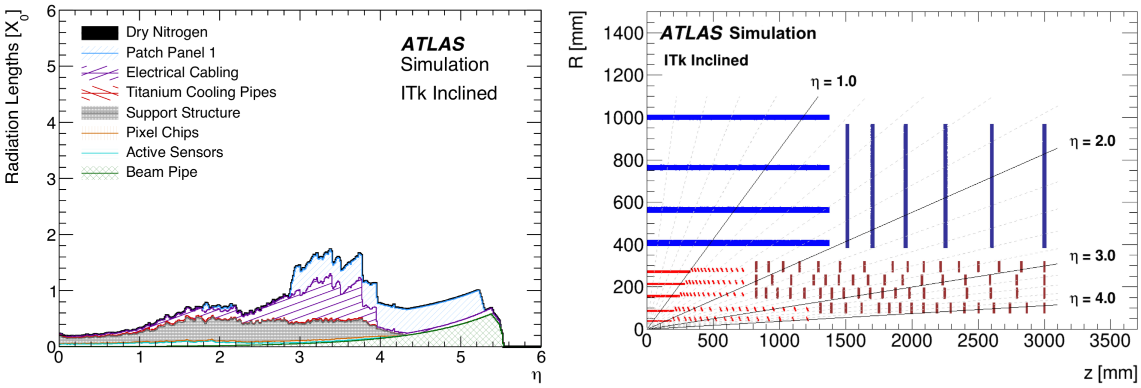

Figure 1: Left: Radiation lengths as a function of pseudorapidity η. The figure shows only positive η since the material distribution is symmetric about $\eta = 0$. Right: ATLAS ITk schematic layout. Only active detector elements in one quadrant are shown. The horizontal axis is the axis along the beam line with zero being the interaction point. The vertical axis is the radius measured from the beam line. The strip part of the ITk is shown in blue. The outer radius is set by the bore of the solenoid. Figures are taken from Ref. [3].

a number of pixel rings, see the right panel of Figure 1. The tracking detector will be surrounded by a polyethylene moderator which decreases the silicon damage arising from the flux of neutrons coming from the calorimeters. Gaps will be preserved between sub-detector parts to allow for supports, services and insertion clearances.

The strip system covers ± 2.7 units of pseudorapidity. The strip barrel extends from -1400 mm to +1400 mm along the z-axis, while the EC disks are located between edge of the strip barrel and $z = \pm 3000$ mm . The radii at which the barrel layers are located and positions of the EC disks on the z-axis are chosen to optimize the number of hits on a track and the p_{T}-resolution. The two inner layers of the barrel are equipped with the short strips of 24.1 mm length. The outer two layers have long strips with 48.2 mm.

The basic mechanical building blocks of the barrel layers and EC disks are staves and petals, respectively. The four barrel layers (L0-L3) consist of 392 staves with modules mounted on both sides, which means 196 staves positioned on each side of $z = 0$. Each barrel stave is populated with 28 modules - 14 on each stave side. The modules on each side of the stave are rotated with respect to the beam line by ± 26 mrad, so the total rotation between the strips on each side of the stave is 52 mrad. Each EC disk is populated with 32 identical petals. Each individual petal has nine modules on each side with six different sensor geometries, corresponding to 6 rings (R0-R5) around the beam axis in different $R\phi$ planes, to cover the wedge shape petal surface. The stereo angle of 20 mrad is directly implemented in the EC sensors to achieve a total stereo angle of 40 mrad.

2.2 ITk Strip sensors

The strips on the silicon sensors chosen for the ATLAS ITk Strip project are AC-coupled with n-type implants in a p-type float-zone silicon bulk (n$^+$-in-p FZ). The main reason for using the n$^+$-in-p technology is the much higher signal after irradiation and the absence of radiation induced type inversion compared with p$^+$-in-n technology used in current SCT detector. On the other side, n$^+$-in-n technology is significantly higher in costs relative to n$^+$-in-p as the required double-sided

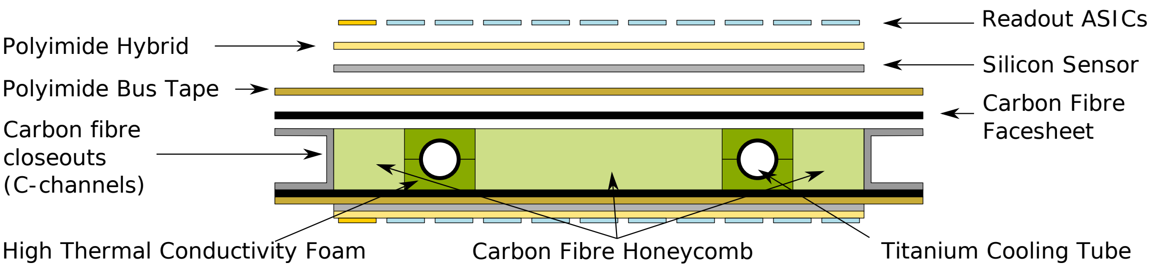

Figure 2: Schematic of the internal structure of the stave core with added silicon sensors and read-out ASICs (not to scale). Glue layers are not shown. Figure is taken from Ref. [3].

processing reduces yield. Bias resistors are implemented by poly-silicon implants and the inter-strip isolation is achieved by p-stop implants, uniform p-spray or their combination. The target thickness of silicon strip sensors is between 300 and 320 μm. The other sensor specifications can be found in Table. 6.1 of Ref. [3].

The barrel sensors have an active area of $\sim 10 \times 10\,\mathrm{cm}^2$. There are 1280 readout strips and the field-shaping strip at each side in parallel to the other strips, giving the constant strip pitch of 75.5 μm. The strips are parallel to the edge of the sensor. The petal sensors require radial strips to give a measurement of the $R\phi$ coordinate. As a result these sensors have a wedge shape with curved edges. The dimensions of the sensors have been chosen to use as few silicon wafers as possible with 32 petals per disk and fully covering the radial range required by the layout. The strip lengths are optimised to keep the strip occupancy below 1%, resulting in varying strip lengths increasing from 19.0 mm in the region closest to the beam axis to 60.1 mm in the outermost region. The EC strip pitch is between 69 and 84 μm depending on the particular sensor type and strip segment, but it is constrained to be as close as possible to the barrel strip pitch at the bond pad region to allow direct wire bonding between the read-out application-specific integrated circuits (ASICs) and the sensor.

2.3 ITk Strip ASICs

A number of custom-made ASICs are being developed for the ATLAS ITk strip system. The most critical ASICs are ATLAS Binary Chip (ABC), Hybrid Controller Chip (HCC), Autonomous Monitor and Control Chip (AMAC) and the bPOL12V chip. The prototype versions of these ASICs have been extensively studied during the evaluation phase of the project, while the production versions will be used for detector construction.

The production ABCStar ASICs will be fabricated at Global Foundries in a 130 nm CMOS technology using standard 8-inch wafers thinned to $200-320$ μm. The chip will be 7.9 mm wide with the maximum length of 6.8 mm. Their main purpose is to convert the charge collected on the individual strips into the hit information. Compared to the daisy-chain readout architecture used for prototype ABC130 ASICs, with data transmitted serially through a group of ABC130 front-end chips to HCC130 chip, the production ABCStar ASICs accommodate a new star architecture with point-to-point connections between each ABCStar and HCCStar ASICs on the read-out PCB board [3]. The ABCStar ASICs provide all functions required for processing of signals from 256 strips of a silicon strip detector employing a binary read-out.

The HCC chip is the interface ASIC between the signalling on the stave and the ABC ASICs.

The chip has stave-side inputs for the beam crossing clock and control signals. These control signals include triggering and general commands. After processing in the HCC, the control signals are sent on a hybrid-side bus to the ABC chips. Any data being returned from the ABC ASICs are sent through the HCC, where they are queued and sent out on the data line on the stave.

The AMAC chip provides both monitoring and interrupt functionality. The monitoring of voltages, temperatures and sensor bias current on the strip modules at a rate of approximately one sample per millisecond is achieved through the improved analogue monitor block from the HCC130 chip.

The chosen powering scheme for the ITk strip modules is based on the distribution of power through on-detector DC-DC converter modules [4], which will be built around the bPOL12V buck converter ASIC, integrating both the power switches and the control circuitry. The bPOL12V converter provides output voltages in the range of 0.6 to 5 V from an input voltage of 5 to 12 V. The output current can be as high as 4 A. The switching frequency can be adjusted in the range from 1 to 3 MHz. The current prototype converter, FEAST, has proved to be radiation tolerant to a total ionization dose greater than 200 Mrad and displacement damage up to 5×10^{14} $\mathrm{n_{eq}/cm^2}$. Whilst the production version of the converter, bPOL12V, is expected to stand displacement damage up to 5×10^{15} $\mathrm{n_{eq}/cm^2}$.

2.4 ITk Strip modules

The basic unit of the ATLAS ITk Strip detector is the silicon strip module. A module consists of one silicon strip sensor, one or two low-mass PCB's, called hybrids, and one power board. Hybrids host between 7 and 12 ABCStar ASICs and one or two HCCStar ASICs. Each power board includes silicon sensor high-voltage (HV) bias filtering circuit, sensor bias HV switch, AMAC ASIC for control and monitoring, and low-voltage DC-DC power block with the radiation tolerant bPOL12V converter ASIC. All the module components are glued together using either UV curable glue, silver-loaded epoxy adhesive or electronics grade epoxy. Connections between ASICs, silicon sensors and electronics are made through ultra-sonic wire bonding.

2.5 Local and Global supports

Local supports - staves and petals - provide mechanical, geometric, thermal and electrical support to modules. The mechanical and cooling performance of the local support is determined by employing high stiffness, high thermal conductivity carbon-fiber for the face-sheets and the sandwich geometry, which gives high rigidity and allows the cooling structures to be buried withing the core such that heat generated by the modules is removed directly, see Figure 2. Geometrically, local supports interface to their global support structures through the series of position locators and locking points, which together define the position of each local support. The electrical services needed to power and control modules are connected to the off-stave services via the end-of-substructure (EoS) card and distributed to each module along electrical connections on the surfaces of the local support core. Similarly, the EoS card receives the data from each module, processes it and then transmits it via optical links to the data acquisition systems.

The primary role of the global support structures is to locate robustly the substructures carrying the strip modules. The global support structures will be largely made of carbon-fiber in order to cope with the large temperature variations up to 60 °C.

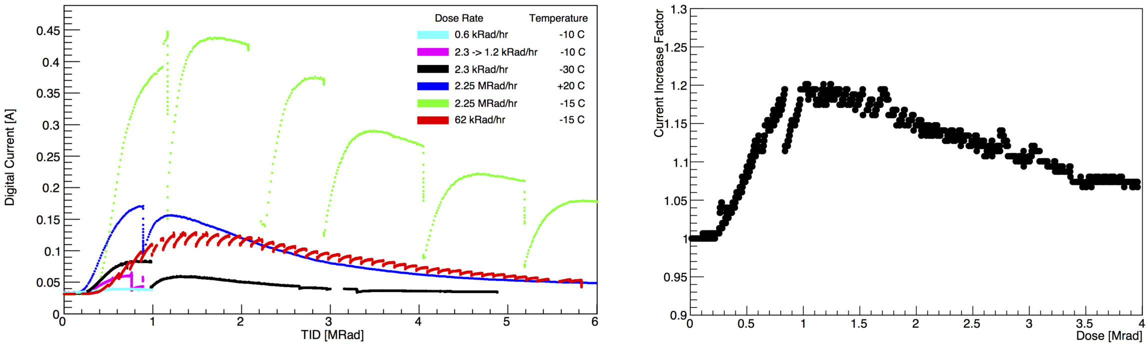

Figure 3: Left: Dependence of ABC130 chip digital current on the total ionization dose during X-ray irradiations at different dose rates and temperatures. Right: Digital current increase factor measured for an HCC130 chip as a function of total ionization dose during the X-ray irradiation. Figures are taken from Ref. [3].

2.6 Overall electronics architecture

Charged particles passing through the sensor create a signal charge within the silicon sensor diode. The signal is transmitted through a wire to the front-end ABCStar chip containing 256 pre-amplifiers and discriminators together with the L0 buffer, event builder and cluster finder. With the ABCStar chip the signal on each channel is amplified, shaped and discriminated to provide the binary output. Every HCCStar chip hosted on the hybrid is able to interface the stave or petal service bus with up to 11 front-end ASICs. The HCCStar receives the signal from the ABCStar, builds packets and moves them on. Trigger, Timing and Control (TTC) signals arriving from the off-detector systems are sent from the EoS to each HCCStar via the TCC bus on the bus tape. The TTC consists of a 40 MHz system clock, a serial command/L0 trigger and R3/L1 trigger.

A power board with LV power converter, HV multiplexer switch (MUX) and AMAC chip connects to the EoS card, which distributes LV and HV power to each hybrid and sensor via a power bus, and Detector Control Signals (DCS) through the I^2C bus. The data lines, TTC bus, power and DCS bus are integrated into a single copper/kapton bus tape that is co-cured onto the stave or petal core. The EoS includes a low power GigaBit Tranceiver (lpGBTx) performing the serialization/deserialization required for data being transmitted and received on the bus tape, and a Versatile link (VTRx+) fibre optics driver [5] for high speed optical transmission and reception between the EoS and the off-detector electronics.

3. System tests

During the extensive R&D programme of the ATLAS ITk Strip project the functionality of each individual component is evaluated and the obtained values are compared with specifications.

3.1 ASIC testing

During the X-ray and proton irradiation studies of ABC130 and HCC130 chip prototypes a significant increase of ASICs digital current was observed, peaking between 1 and 2 Mrad of total ionization dose. As shown in Figure 3, this increase depends on the dose rate and temperature

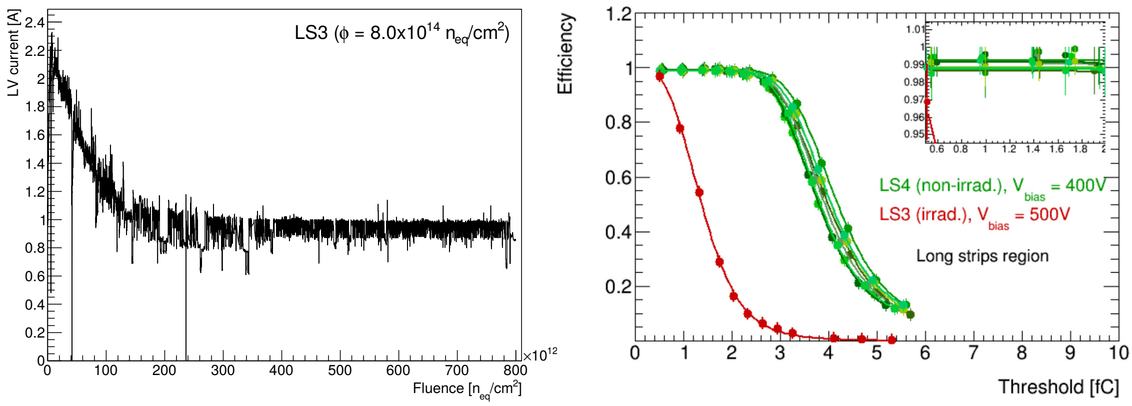

Figure 4: Left: Low-voltage digital current of the hybrid as a function of total proton fluence displayed in n_{eq}/cm^2 for LS3 module during the irradiation at CERN IRRAD facility. Right: The efficiency versus the threshold for seven ASICs on the non-irradiated long-strip module LS4 and one ASIC on the irradiated module LS3. Figures are taken from Ref. [3].

during the irradiation. This effect has its origin in the competing between two main radiation damage mechanisms on deep sub-micron CMOS technologies: the radiation-induced positive charge trapping in the shallow-trench-on-insulator oxide at the edge of the transistor, and the creation of interface states in the dangling bonds between that oxide layer and the silicon [6, 7]. While the build-up of positive charge is relatively fast, the formation of interface states is a slower process. The negative charge trapped in the interface states thus starts to compete with the oxide-trapped charge with a delay which produces the so called rebound effect, observed also in the ATLAS IBL detector [8]. Proton and X-ray irradiation studies done for HCC130 ASICs show that with respect to ABC130 the digital current increase is significantly lower as the HCC130 ASICs contain fewer memory blocks, see the right plot of Figure 3. The higher current increase is expected for HCCStar ASICs with the added memory in the star architecture.

3.2 Test beam and irradiation

Between 2015 and 2017 eight different prototype modules have been tested. These were LS2, LS3 and LS4 modules, which are the full-sized barrel modules with both long and short strips, SS1 short strip barrel module with and without the power board, R0 EC module and two mini-assemblies DAQload10 and DAQload13 using the miniature sensors. From these modules the LS3 detector was fully irradiated by protons to the total fluence of 8.0×10^{14} n_{eq}/cm^2, corresponding to the highest fluence to be delivered to ATLAS ITk Strip detector at HL-LHC, while the DAQload13 module included two miniature sensors irradiated by neutrons to 2×10^{15} n_{eq}/cm^2 and one ABC130 ASIC X-ray irradiated to the total ionization dose of 4 MRad with the rate of 0.85 MRad/hr at -5 °C.

The LS3 module was irradiated at the CERN IRRAD facility with 24 GeV protons produced by CERN Proton Synchrotron accelerator resulting in both ionizing (TID) and non-ionizing energy loss (NIEL) damage. During the irradiation, the module was mounted in the cooling box and the movable stage allowed scanning of the sample to uniformly irradiate the full sensor area. The de-

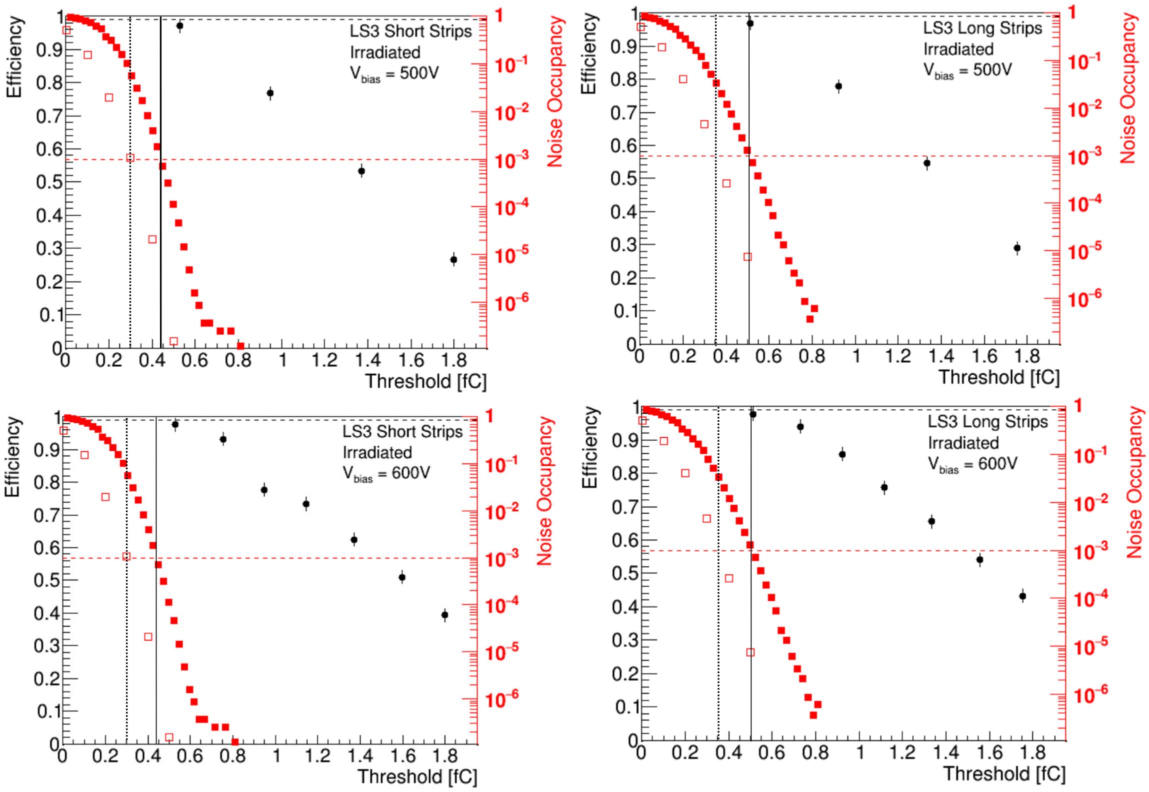

Figure 5: The signal efficiency (black dots) compared to the noise occupancy at different thresholds for the ABC130 (full red squares) and ABCStar (open red squares) ASICs. Left plots correspond to the short strips while the right plots to the long-strips of the irradiated LS3 module. Two upper plots show data measured with the sensor bias voltage of 500 V and the bottom two plots correspond to the sensor bias voltage of 600 V. Figures are taken from Ref. [3].

vice was cooled down to -20 °C, the sensor was not biased and the chips were powered, configured and clocked, and digital current was monitored for the whole irradiation period of 19 days. The measured values of digital current as a function of total proton fluence are shown on the left panel of Figure 4, where the LV current increase discussed in Sec. 3.1 is clearly visible.

A test beam at CERN allowed us to compare the performance of full-sized barrel module before and after irradiation to 8.0×10^{14} n_{eq}/cm^2. The right panel of Figure 4 shows the efficiency curves for long-strip regions of seven ASICs of the non-irradiated LS4 module and for one ASIC of the irradiated module LS3. As expected the charge collection is significantly reduced after the irradiation.

At the end-of-lifetime, modules are required to have a detection efficiency higher than 99% at the thresholds that allow for operation with less than 1×10^{-3} channel noise occupancy. It has been shown that requiring a signal-to-noise ratio of 10:1 will simultaneously satisfy these efficiency and noise occupancy requirements. Figure 5 shows the signal efficiency at the irradiated LS3 module studied at CERN test beam. Prior to irradiation a wide range of thresholds between 0.5 and 2.0 fC meet both the noise occupancy and hit efficinecy requirements. With the irradiation the range of thresholds which will simultaneously meet both requirements is significantly reduced. A decrease of the measured signal is caused by the combination of the lower substrate resistance of the tested ATLAS12 sensor and the lack of annealing after the irradiation. Also the noise in the prototype chips ABC130 is larger than expected in the production chip ABCStar. For comparison, the noise occupancy data extrapolated from the equivalent noise charge measurements of the ABCStar front-end is added to the Figure 5. With the reduced noise in the production chips the range of thresholds that meet the specifications on noise occupancy and efficiency will be much wider.

4. Conclusions

The production of the ATLAS ITk Strip detector involves both a range and quantity of objects that far exceed the production of current SCT. The total number of 10,976 barrel and 6,912 EC ITk strip modules has led to improving in every way the ease of construction and affordability during the production phase. This effort to streamline the assembly process has driven the development of the local support concept where groups of 28 barrel modules will be mounted onto the stave and groups of 18 EC modules onto each EC petal. These local support structures form independent and functional sub-systems which can be fully tested before being installed in the global structure. This ensures a highly parallelized workflow and that the time between the start of the assembly of a particular module to a test in its final operational environment is as small as possible.

Acknowledgments

We thank for the support of the Ministry of Education, Youth and Sports of the Czech Republic coming from the project LM2015058 - Research infrastructure for experiments at CERN.

References

[1] The ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, JINST **3**, S08003 (2008).

[2] The ATLAS Collaboration, *Letter of Intent for the Phase-II Upgrade for the ATLAS Experiment*, CERN-LHCC-2012-022, LHCC-I-023, CERN (2012).

[3] The ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Strip Detector*, CERN-LHCC-2017-005, ATLAS-TDR-025, CERN (2017).

[4] A. Affolder *at al.*, *DC-DC converters with reduced mass for trackers at the HL-LHC*, Journal of Instrumentation **6**, C11035 (2011).

[5] The CMS Collaboration, *The versatile link, a common project for super-LHC*, Journal of Instrumentation **4**, P12003 (2009).

[6] F. Faccio and G. Cervelli, *Radiation-induced edge effects in deep submicron CMOS transistors*, IEEE Transactions on Nuclear Science **52**, 2413 (2005).

[7] F. Faccio *et al.*, *Total ionizing dose effects in shallow trench isolation oxides*, Microelectronics Reliability **48**, 1000 (2008).

[8] A. La Rosa *et al.*, *Radiation induced effects in the ATLAS Insertable B-Layer readout chip*, ATL-COM-INDET-2016-082, CERN (2016).